

IN THE SPECIFICATION

Please amend Specification page 4, ¶ 2, lines 15-19 as set forth below.

"Referring to FIG. 1D, the dummy gate, exposed by CMP, is removed. Now referring to FIG. 1E, a gate insulating layer 8 is then formed along a surface of the resultant structure. Subsequently, a gate metal layer 9, such as a tungsten layer, is deposited on the gate insulating layer 8."

Please amend Specification page 5, ¶ 2 (lines 4-12) as set forth below.

"In a semiconductor fabrication process, a device isolation process has to precede the gate electrode formation and a gate electrode line traverses active and field areas simultaneously. As shown in FIG. 2, the surface of a field oxide layer 11 is generally higher than the surface of the semiconductor substrate 1 in the active area **t** in the device isolation process. Thus, a step difference **a** shown in FIG. 2 as the gap between the top portion of the field oxide layer 11 defining the field area **h** (FIG. 2) and the top portion of the semiconductor substrate, a mid-portion of which is defined as the active area **t** is generally between 200 to 500 Å."